

REMARKS

Applicant appreciates the Examiner's consideration and entry of Applicant's Amendment filed June 3, 2004 and the continued indication of the potential allowability of Claims 5, 6, 10 and 16. Applicant respectfully requests reconsideration and withdrawal of the rejections of Claims 1, 4, 7, 7-9, 11-15, 17-20 and 22 for the reasons provided in the Amendment of June 13, 2004 (incorporated by reference in the interest of brevity), as supplemented by further remarks provided herein.

Independent Claims 1, 14 and 20 stand rejected as anticipated by Hynecek. Applicant has pointed out that Hynecek shows an ohmic (conductive), and not a capacitive, coupling between the output of the alleged "feedback circuit," which is identified in the final Office Action as "circuit path beginning at the drain of the circuit 50 and ending at the drain of circuit 52, wherein the path is intercepted with a power source VDD and a resistor 64." Final Office Action, p. 5. In response to this argument, the final Office Action appears to assert that Miller capacitance associated with the transistor 52 provides the capacitive coupling recited in Claim 1. Applicant respectfully traverses this reasoning, as the Office Action appears to misinterpret the discussion of Miller capacitance provided in Hynecek and, thus, draws erroneous conclusions regarding the teachings of this reference.

In the circuit illustrated in FIG. 2 of Hynecek, a source follower circuit includes an input NMOS transistor 52 and a load transistor 54. As is well known in the art, in such a configuration, a Miller effect would occur between the *gate and drain* terminals of the NMOS transistor 52. In particular, in the source-follower configuration shown in FIG. 2 of Hynecek, the Miller effect would cause a parasitic capacitance between the gate and drain terminals of the transistor 52 to be effectively increased (by an amount representing the "Miller capacitance") due to the inverse dependence of the voltage of the drain on the voltage of the gate in this configuration, which causes voltages at the "terminals" of the gate-to-drain parasitic capacitance to change in opposite directions simultaneously.

The cited passage from Hynecek (column 2, lines 27-32) explains that the PMOS transistor 50 connected to the output of the source follower circuit in FIG. 2 can compensate for this Miller effect by providing positive feedback to the drain of transistor 52. In

In re: Sang-sik Park
Serial No.: 09/399,995
Filed: September 20, 1999
Page 8 of 9

particular, the positive feedback provided by the PMOS transistor 50 acts to reduce voltage excursions of the drain of the transistor 52 responsive to changes in the gate voltage of the transistor 52, which can reduce the Miller effect, i.e., reduce the Miller capacitance.

The Miller capacitance in FIG. 2 of Hynecek does not capacitively couple the output of the feedback circuit (which, in the description in the final Office Action, appears to be the node where the drain of the transistor 50 is coupled to the resistor 64) to the bias terminal of the source follower circuit (which, in the description provided in the final Office Action, is the drain terminal of the transistor 52). Rather, as noted above, *the Miller capacitance in the circuit of FIG. 2 of would occur between the gate terminal of the transistor 52 and the drain terminal of the transistor 52*. As Applicant has pointed out, the coupling between the output of the alleged feedback circuit is ohmic (conductive) and not capacitive, as the latter would involve some sort of intervening dielectric between the nodes in question, and no such dielectric is shown in the circuit of FIG. 2 of Hynecek. Accordingly, the cited material from Hynecek does not provide the teachings alleged in the final Office Action, and does not disclose or suggest all of the recitations of Claim 1. Applicant, therefore, respectfully requests that the rejection of Claim 1 be withdrawn. Applicant further submits that similar arguments support the patentability of independent Claims 14 and 20 over Hynecek, and requests that the rejections of these claims be withdrawn.

Applicant submits that the claims are in condition for allowance for at least the reasons provided in the Amendment of June 13, 2004 and the foregoing remarks. Accordingly, Applicant respectfully requests allowance of the claims and passing of the application to issue in due course. Applicant encourages the Examiner to contact the undersigned by telephone for resolution of any remaining issues.

Respectfully submitted,



Robert M. Meeks
Registration No. 40,723

In re: Sang-sik Park
Serial No.: 09/399,995
Filed: September 20, 1999
Page 9 of 9

RECEIVED

SEP 29 2004

Technology Center 2600

USPTO Customer No. 20792
Myers Bigel Sibley & Sajovec
Post Office Box 37428
Raleigh, North Carolina 27627
Telephone: 919/854-1400
Facsimile: 919/854-1401

Certificate of Mailing under 37 CFR 1.8 (or 1.10)

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on September 23, 2004.

Candi L. Riggs
Candi L. Riggs